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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Filing Date	1/31/02
				First Named Inventor	Steven Telg, et al.
				Group Art Unit	2811
				Examiner Name	Belu M. Dick
Sheet	1		1	Attorney Docket Number	SPLX.P0097

U.S. PATENT DOCUMENTS						
Examiner Initials	Cite No. ¹	U.S. Patent Document Number	Kind Code ² (if known)	Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
bmc	1.	5,519,630		05-21-1996	Nishiyama et al.	RECEIVED DEC 08 2003 Technology Center 2100
	2.	5,537,341		07-16-1996	Rose et al.	
	3.	5,696,974		12-09-1997	Agrawal et al.	
	4.	5,574,441		05-19-1998	Tokunoh et al.	
	5.	5,787,010		07-28-1998	Schaefer et al.	
	6.	6,023,566		02-08-2000	Belkhale et al.	
	7.	6,301,696	B1	07-09-2001	Lien et al.	

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
bmc	8.	Crastes, M. et al., A Technology Mapping Method Based on Perfect and Semi-Perfect Matchings, Design Automation Conference, 1991, 28 th ACM/IEEE, June 17-21, 1991, pp. 93-98.	
bmc	9.	Devadas, S. et al., Synthesis and Optimization for robustly delay-fault testable combinational logic circuits, Design Automation Conference, 1990, 27 th ACM/IEEE, June 24-28, 1990, pp. 221-227.	

Examiner Signature	Belu M. Dick	Date Considered	12/8/02
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